PATENT ABSTRACTS OF JAPAN

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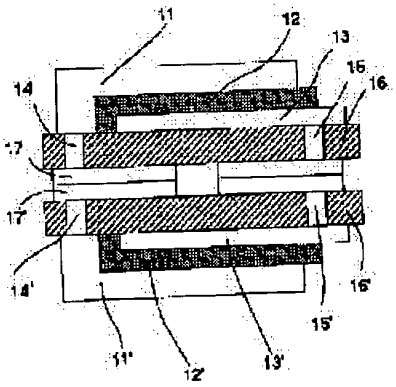
(54) THIN-TYPE LAMINATED CAPACITOR

(57)Abstract:
PROBLEM TO BE SOLVED: To manufacture a laminated capacitor which is thin, high in flexual strength, and large in capacity by a method wherein a thin capacitor is composed of a first electrode layer and a second electrode layer both formed on a silicon wafer, the electrode layers are connected to junction electrodes provided in the rear of the silicon wafer through the intermediary of through-holes provided to the silicon wafer, and two of the thin capacitors are joined together by bonding the junction electrodes aligning them with each other.
SOLUTION: A thin film capacitor is composed of a first electrode layer 11 and a second electrode layer 13 both formed on the surface of a silicon wafer 16, the electrode layers 11 and 13 are connected to junction electrodes 17 provided in the rear of the wafer 16 through the intermediary of through-holes 14 and 15 provided to the wafer 16, and the two thin film capacitor of the same structure are joined together joining the junction electrodes 17 together aligning them with each other. That is, the thin capacitor is composed of the upper electrode layer 11, a dielectric layer 12, and a lower electrode layer 13, the electrode layers 11 and 13 are connected to the junction electrodes 17 provided in the rear of the silicon wafer 16 through the intermediary of the through-holes 14 and 15, and the thin capacitors of the same structure are joined together into a two-layered thin film laminated capacitor by bonding the junction electrodes 17 of them together.



LEGAL STATUS

[Date of request for examination]

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[Date of final disposal for application]

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10-004,030 A

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CLAIMS

[Claim(s)]
[Claim 1] It has the 1st electrode layer and the 2nd electrode layer on the silicon wafer principal plane, and a dielectric layer is between the 1st electrode layer and the 2nd electrode layer. The 1st electrode layer and the 2nd electrode layer by the breakthrough which was able to be opened in the silicon wafer, respectively The thin shape multilayer capacitor characterized by carrying out alignment of the junction electrode of the thin shape capacitor which the thin shape capacitor of the structure where a junction electrode is taken, respectively is in a silicon rear face, and has other same structures in it, and joining.
[Claim 2] It has the 1st electrode layer and the 2nd electrode layer on the silicon wafer principal plane, and a dielectric layer is between the 1st electrode layer and the 2nd electrode layer. The 1st electrode layer and the 2nd electrode layer by the breakthrough which was able to be opened in the silicon wafer, respectively At the silicon rear face A lower junction electrode Each Similarly with ****** structure That alignment of the junction electrode of the thin shape capacitor which there is a thin shape capacitor of structure with the up junction electrode connected to the 1st electrode layer and the 2nd electrode layer also on the surface of a principal plane, and has other same structures is carried out, and the up electrode of a thin shape capacitor different from the lower electrode of one thin shape capacitor joins The thin shape multilayer capacitor by which it is characterized.
[Claim 3] The junction electrode of a thin shape capacitor is the thin shape multilayer capacitor of the claim 1 characterized by being joined after cleaning a front face by the neutral atom of an argon beforehand, and a claim 2.
[Claim 4] The structure by the side of the above-mentioned principal plane is the thin shape multilayer capacitor of the claim 1 characterized by being made thin bordering on the inner layer oxide-film layer of a silicon on insulator after being formed using a SHIRIOKON-on insulator wafer, or a claim 2.
[Claim 5] The aforementioned dielectric layer is the thin shape multilayer capacitor of the claim 1 which is formed of barium strontium titanium oxide or PZT, and is characterized by things, or a claim 2.
[Claim 6] The capacitor which carries out a laminating is a thin shape multilayer capacitor of the claim 2 characterized by dividing and carrying out the laminating of the one wafer.
[Claim 7] The thin shape multilayer capacitor of the claim 2 which carries out the laminating of the capacitor of the same number of layers, and is made into the number of layers of double precision.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention is invention about a multilayer capacitor strong against bending in a thin shape.
[0002]
[Description of the Prior Art] The conventional technology is described to 517 pages etc. from the electronic-intelligence communication handbook (the Ohm-Sha Ltd. issue April, 1990 30 1st edition 2nd ****** per day) 516. This structure is shown in drawing 3 . With this structure, it has become as it is shown in the cross section which sintered the dielectric ceramics which makes titanium oxide etc. the main material, and carried out the laminating of the 1st ceramic layer 32, the 2nd ceramic layer 33, and the 3rd ceramic layer 34 to the multilayer in the example of drawing 3 . The electrode 35 other than an electrode 31 is attached in right and left.
[0003]
[Problem(s) to be Solved by the Invention] Although it is possible to make thickness of the ceramic of this each class thin to about 50 microns, since the coarse particle has joined together, a ceramic will break simply in **** with it etc. extremely. [large defect density and] [slight] Therefore, thickness cannot bear bending in the thin shape IC card of which 200 microns or less are required.
[0004]
[Means for Solving the Problem] 1st means to solve the above-mentioned technical problem has the 1st electrode layer and the 2nd electrode layer on the silicon wafer principal plane, and a dielectric layer is between the 1st electrode layer and the 2nd electrode layer. The 1st electrode layer and the 2nd electrode layer by the breakthrough which was able to be opened in the silicon wafer, respectively It is considering as the thin shape multilayer capacitor characterized by carrying out alignment of the junction electrode of the thin shape capacitor which the thin shape capacitor of the structure a junction electrode's being taken, respectively is in a silicon rear face, and has other same structures in it, and joining.
[0005] 2nd means to solve the above-mentioned technical problem has the 1st electrode layer and the 2nd electrode layer on the silicon wafer principal plane, and a dielectric layer is between the 1st electrode layer and the 2nd electrode layer. The 1st electrode layer and the 2nd electrode layer by the breakthrough which was able to be opened in the silicon wafer, respectively At the silicon rear face A lower junction electrode Each Similarly with ****** structure That alignment of the junction electrode of the thin shape capacitor which there is a thin shape capacitor of structure with the up junction electrode connected to the 1st electrode layer and the 2nd electrode layer also on the surface of a principal plane, and has other same structures is carried out, and the up electrode of a thin shape capacitor different from the lower electrode of one thin shape capacitor joins It is considering as the thin shape multilayer capacitor by which it is characterized.
[0006] 3rd means to solve the above-mentioned technical problem is considering as the thin shape multilayer capacitor of the claim 1 characterized by joining it after the junction electrode of a thin shape capacitor cleans a front face by the neutral atom of an argon beforehand, and a claim 2.
[0007] It is making 4th means solving the above-mentioned technical problem into the thin shape multilayer capacitor of the claim 1 characterized by making it thin bordering on the inner layer oxide-film layer of a silicon on insulator after the structure by the side of the above-mentioned principal plane is formed using a SHIRIOKON-on insulator wafer, or a claim 2.
[0008] The dielectric layer of the above [5th means to solve the above-mentioned technical problem] is considering as the thin shape multilayer capacitor of the claim 1 which is formed of barium strontium titanium oxide or PZT, and is characterized by things, or a claim 2.
[0009] The capacitor which carries out the laminating of 6th means to solve the above-mentioned technical problem is considering as the thin shape multilayer capacitor of the claim 2 characterized by dividing and carrying out the laminating of the one wafer. 7th means to solve the above-mentioned technical problem is considering as the thin shape multilayer capacitor of the claim 2 which carries out the laminating of the capacitor of the same number of layers, and is made into the number of layers of double precision.
[0010]
[Embodiments of the Invention] Drawing 1 shows the example of this invention. Drawing 1 shows the cross section which carried out facing-each-other junction of the thin shape capacitor of two sheets. The capacitor consists of the up electrode layer 11, a

dielectric layer 12, and a lower electrode layer 13. A lower electrode layer is taken out for an up electrode layer as a junction electrode 17 at the rear face of silicon 16 by the lower electrode through hole 15 by the up electrode through hole 14 again. A two-layer thin shape multilayer capacitor is formed by connecting these junction electrodes. The thickness of silicon is about 50 micron m from 0.1-micron meter. If this is generally described, it has the 1st electrode layer and the 2nd electrode layer on the silicon wafer principal plane, and a dielectric layer is between the 1st electrode layer and the 2nd electrode layer. The 1st electrode layer and the 2nd electrode layer by the breakthrough which was able to be opened in the silicon wafer, respectively The junction electrode of the thin shape capacitor which the thin shape capacitor of the structure where a junction electrode is taken, respectively is in a silicon rear face, and has other same structures in it serves as a thin shape multilayer capacitor characterized by carrying out alignment and joining. Since a base material uses silicon with very high purity, manufacture of a capacitor strong against bending is attained.

[0011] Drawing 2 shows another example of this invention. The thin shape capacitor consists of the up electrode layer 25, a dielectric layer 26, and a lower electrode layer 23 like drawing 1 . An up electrode layer lower junction electrode 29a Uses a lower electrode layer as the rear face of silicon 28 by the through hole again, and it is taken out by the silicon section through hole 29. A lower electrode layer is taken out for the up electrode layer 25 by the lower electrode up through hole 27 by the up junction electrode 22 with the up electrode up through hole 21 to an up junction electrode. Alignment of the lower junction electrode 29a is carried out to another up junction electrode of another thin shape capacitor, and it is joined to it. A two-layer thin shape multilayer capacitor is formed by connecting these junction electrodes. If this is generally described, it has the 1st electrode layer and the 2nd electrode layer on the silicon wafer principal plane, and a dielectric layer is between the 1st electrode layer and the 2nd electrode layer. The 1st electrode layer and the 2nd electrode layer by the breakthrough which was able to be opened in the silicon wafer, respectively At the silicon rear face A lower junction electrode Each Similarly with ****** structure That alignment of the junction electrode of the thin shape capacitor which there is a thin shape capacitor of structure with the up junction electrode connected to the 1st electrode layer and the 2nd electrode layer also on the surface of a principal plane, and has other same structures is carried out, and the up electrode of a thin shape capacitor different from the lower electrode of one thin shape capacitor joins It becomes the thin shape multilayer capacitor by which it is characterized.

[0012] Drawing 4 shows the process flow for invention carrying out. Drawing 4 (a) shows the cross section immediately after the process which attached the lower electrode layer on the silicon wafer with an oxide film. Drawing 4 (b) shows the cross section immediately after the process which adhered the dielectric layer. This dielectric layer is formed of barium strontium titanium oxide or PZT, and is characterized by things. A property is not changed even if the barium strontium titanium oxide film or PZT film of this invention has bending which the usual card will bend, namely, will allow the variation rate of 20cm by the longitudinal direction of a card if it is for 0.01 to 10 microns, respectively. Drawing 4 (c) shows the cross section immediately after the process which adhered the up electrode layer. Drawing 4 (d) shows the cross section immediately after the process which made the silicon wafer thin. A wafer can be made thin to stability to 0.1-micron meter, if it is made thin bordering on the inner layer oxide-film layer of a silicon on insulator after being formed using a SHIRIOKON-on insulator wafer. It is because only silicon can be alternatively **********ed if a potassium hydroxide is used for ETCHIGGU liquid. Drawing 4 (e) shows the cross section which carried out opening of the lower electrode through hole 46 and the lower electrode through hole 47 to the silicon wafer 45 made thin by etching. Drawing 4 (f) shows the cross section in which the up electrode layer junction electrode 48 and the lower electrode junction electrode 49 were formed.

[0013] Drawing 5 shows the process which this invention joins. With the neutral argon atom 52, the upper thin shape capacitor 51 and the lower thin shape capacitor 53 are joined, after the junction electrode of a thin shape capacitor carries out clean NINGU of the front face by the neutral atom of an argon beforehand. It does not become thick, even if a glue line will be made very thinly with 1 micron from 0.1 microns and will make it a multilayer capacitor, if it does in this way. Moreover, since it can paste up at a room temperature, there is no contraction by thermal expansion and the multilayer capacitor excellent in reliability can be realized.

[0014] Drawing 6 shows the example of a form of operation of this invention. Drawing 6 (a) shows the wafer plan 61 with a thin shape capacitor, and the wafer plan 62 with a thin shape capacitor. Drawing 6 (b) shows the plan 63 and cross section 64 of a capacitor which carried out 2 chip boxes of the wafer, and were joined. Drawing 6 (c) shows the plan 65 and cross section 66 of a capacitor which carried out the quarto further and which were joined. The thin shape multilayer capacitor of the capacitor which carries out a laminating which carries out the laminating of the capacitor of the same number of layers as the thin shape multilayer capacitor characterized by dividing and carrying out the laminating of the one wafer, and is made into the number of layers of double precision becomes possible.

[0015] Drawing 7 shows the example which carried this invention in the flexible IC card. Drawing 7 (a) shows the cross section of the card carried so that the coils 74 and 0.1 with a thin shape of 200 micrometers to 200-micrometer thin shape semiconductor chip 76 may bend from these multilayer capacitors 71 and 0.1 together with the substrate which inserted the 200-micrometer thin shape semiconductor chip 76 in the neutral plane 72 of the card substrate 75, and bent it from the coils 74 and 0.1 with a thin shape of 200 micrometers from multilayer capacitors 71 and 0.1. Drawing 7 (b) shows the plan of drawing 7 (a).

[0016] Drawing 8 shows the plan of this invention example shown in the cross section of drawing 1 .

[0017] Drawing 9 shows what carried the multilayer capacitor of this invention in the radio card of battery loess, drawing 9 (a) is a plan and drawing 9 (b) shows the cross section of drawing 9 (a). The hole for a through hole 96 tying with the coil pattern 98, and short-circuiting a pattern 95 is shown, and an electrode is pulled out to the coil drawer pattern 97. This coil pattern is formed by screen-stencil and etching technology of a silver paste.

[0018] An electroconductive glue 91 connects the up electrode 11 and the coil end-connection child 93 of a multilayer capacitor. Electroconductive glues may be the anisotropy electric conduction adhesives which distributed the conductive particle to the insulating material. On the card substrate 94, the coil portion 92 formed of the printing-technique exists.
[0019] Drawing 10 shows the cross section of the process which builds a coil and a capacitor into a card. Drawing 10 (a) shows the cross section of a card substrate. Drawing 10 (b) shows the cross section which printed the coil pattern for electrical conducting materials, such as a silver paste, by screen-stencil etc. Drawing 10 (c) shows the cross section of the process immediately after printing a conductive binder. Drawing 10 (d) is showing the cross section immediately after the process which pasted up the multilayer capacitor 101. The structure of this multilayer capacitor 101 has the same structure as the multilayer capacitor shown in drawing 1 . Drawing 10 (e) shows the cross section immediately after the process of the card which pasted up the card cover sheet 102 with adhesives 103, and was completed.
[0020]
[Effect of the Invention] this invention has the 1st electrode layer and the 2nd electrode layer on the silicon wafer principal plane as the claim 1, and a dielectric layer is between the 1st electrode layer and the 2nd electrode layer. The 1st electrode layer and the 2nd electrode layer by the breakthrough which was able to be opened in the silicon wafer, respectively The thin shape multilayer capacitor characterized by carrying out alignment of the junction electrode of the thin shape capacitor which the thin shape capacitor of the structure where a junction electrode is taken, respectively is in a silicon rear face, and has other same structures in it, and joining is proposed. According to the capacitor of such composition, it becomes possible to obtain the capacitor which is a thin shape and can be bent with large capacity like a 10 to 100micro farad at least about 50 microns from thickness 1. The large capacity of this benefits possible the structure which makes a laminating the capacitor formed in silicon with a thin shape, and the effect of bringing about realization of thin shape cards, such as a flexible IC card, is acquired. The composition of a flexible IC card is concretely shown in drawing 7 , and the composition which carried the multilayer capacitor of this invention in drawing 9 is shown. With the card of the composition of such drawing 9 , a part of electric composition of storing energy in a tank by the coil and the capacitor is made. Since a coil is constituted in the shape of printing at this time, number of turns are limited, it is difficult to realize a large inductance and it needs a thin capacitor with large capacity. If a card with a capacitor mass with such a thin shape is realizable, since it will become easy to store the energy by the electromagnetic wave compared with the former, the thing of 5 to 10cm distance becomes that even 15 to 500cm distance can store the energy to which a card can operate by battery loess, and the former can make the application range large.
[0021] When the conventional ceramic condenser was made thin to about 50 microns, it was simply divided in stress, and there was no capacitor mass with a thin shape. With the conventional ceramic condenser, although simply divided in the radius of curvature of 100 millimeters, by the multilayer capacitor of this invention, it is not divided until it becomes 10 millimeters or less, and the very remarkable invention effect is brought about. In this invention, the laminating of the capacitor is produced and carried out on a wafer. A wafer is made thin and it joins by metaled solid phase diffusion welding. The up-and-down breakthrough was able to take out with the thin shape the effect that a mass capacitor strong against bending could be manufactured, by making silicon thin and opening it by etching.
[0022] Since the multilayer capacitor of this invention can realize a mass capacitor with a thin shape in a small area and it is a small area, since it is a thin shape, the capacitor parts which were fit for bending at the thin flexible IC card with sufficient ** can be offered economically with the sufficient yield.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The example of this invention is shown.
[Drawing 2] Another example of this invention is shown.
[Drawing 3] The structure of the conventional capacitor is shown.
[Drawing 4] The operation flow of this invention is shown.
[Drawing 5] The operation flow of this invention is shown.
[Drawing 6] How to produce a multilayer capacitor from a wafer is shown.
[Drawing 7] Another example of this invention is shown.
[Drawing 8] Another example of this invention is shown.
[Drawing 9] Another example of this invention is shown.
[Drawing 10] Another example of this invention is shown.
[Description of Notations]
11 -- Up electrode layer
12 -- Dielectric film layer
13 -- Lower electrode layer
14 -- Up electrode through hole
15 -- Lower electrode through hole
16 -- Silicon
17 -- Junction electrode
21 -- Up electrode up through hole
22 -- Up junction electrode
23 -- Lower electrode layer
24 -- Insulating membrane layer
25 -- Up electrode layer
26 -- Dielectric film layer
27 -- Lower electrode up through hole
28 -- Silicon
29 -- Silicon section through hole
29a -- Lower junction electrode
29b -- Another up junction electrode
31 -- Electrode
32 -- The 1st ceramic layer
33 -- The 2nd ceramic layer
34 -- The 3rd ceramic layer
35 -- Another electrode
41 -- Silicon wafer with an oxide film
42 -- Lower electrode layer
43 -- Dielectric layer
44 -- Up electrode layer
45 -- Silicon wafer made thin
46 -- Up electrode through hole
47 -- Lower electrode through hole
48 -- Up electrode layer junction electrode
49 -- Lower electrode layer junction electrode
51 -- Upper thin shape capacitor
52 -- Neutral argon atom
53 -- Lower thin shape capacitor
61 -- Wafer plan with a thin shape capacitor

62 -- Wafer cross section with a thin shape capacitor
The capacitor plan which carried out the 63--two chip box
The capacitor cross section which carried out the 64--two chip box
65 -- Capacitor plan which carried out the quarto
66 -- Capacitor cross section which carried out the quarto
71 -- Laminating NDENSA
72 -- Neutral plane
74 -- Coil
75 -- Card substrate
76 -- Thin shape semiconductor chip
91 -- Electroconductive glue
92 -- Coil portion
93 -- Coil end-connection child
94 -- Card substrate
95 -- Bond pattern
96 -- Through hole
97 -- Coil drawer pattern
98 -- Coil pattern
101 -- Multilayer capacitor
102 -- Card cover sheet
103 -- Adhesives.

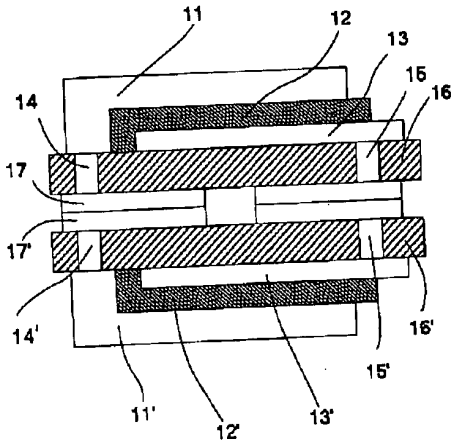
[Translation done.]

* NOTICES *

DRAWINGS

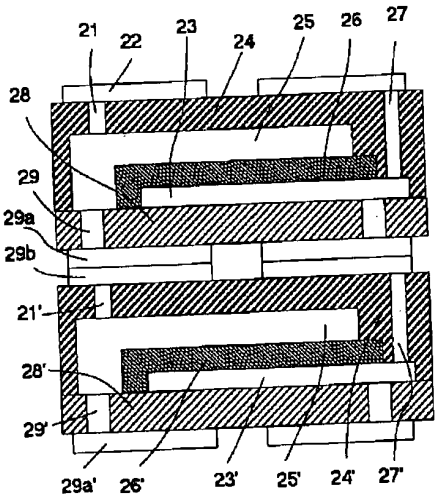
[Drawing 1]

図1



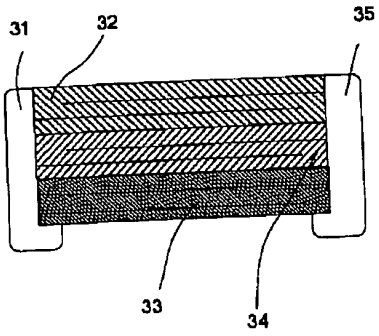
[Drawing 2]

図2



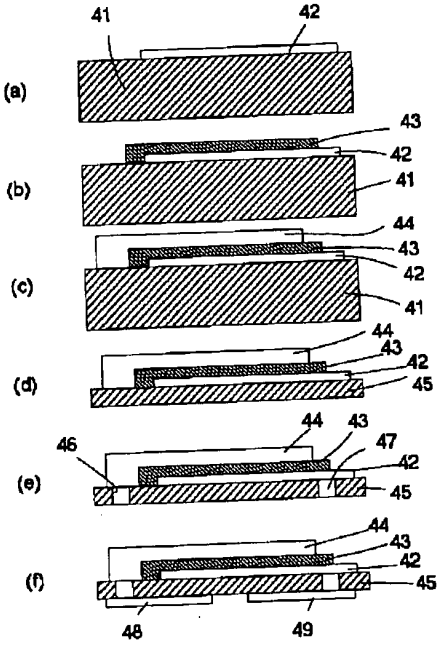
[Drawing 3]

図3



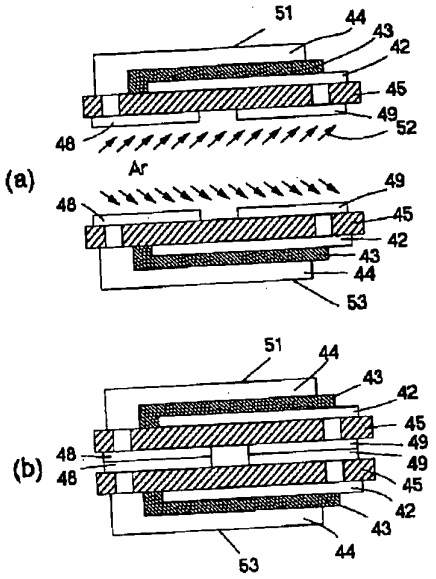
[Drawing 4]

図4



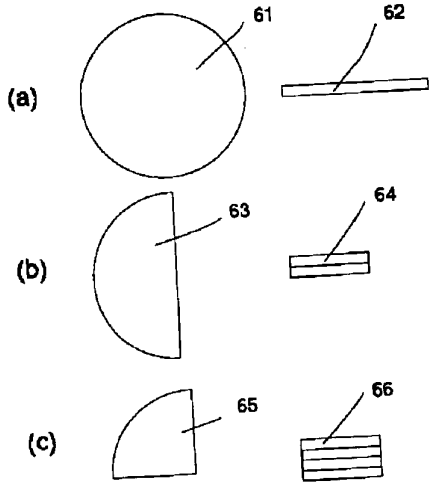
[Drawing 5]

図5



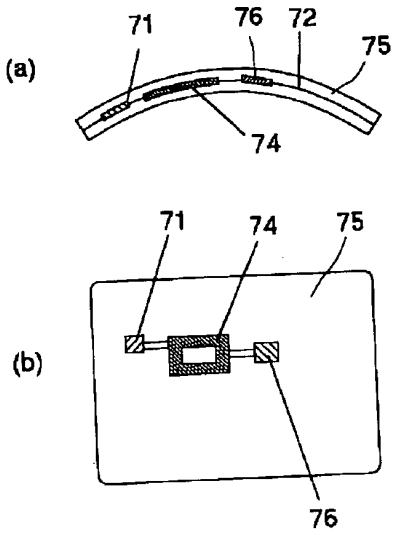
[Drawing 6]

図6



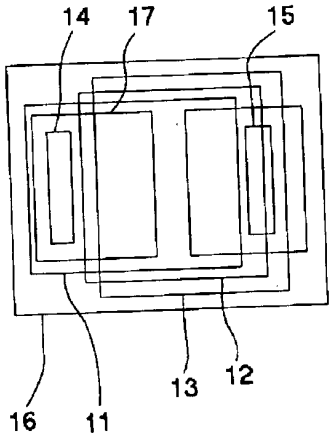
[Drawing 7]

図7



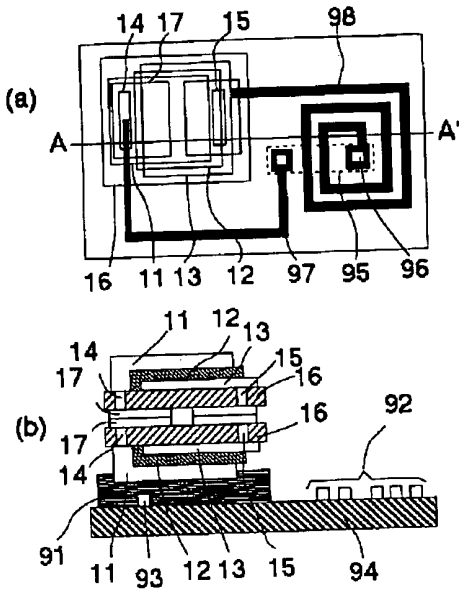
[Drawing 8]

図8



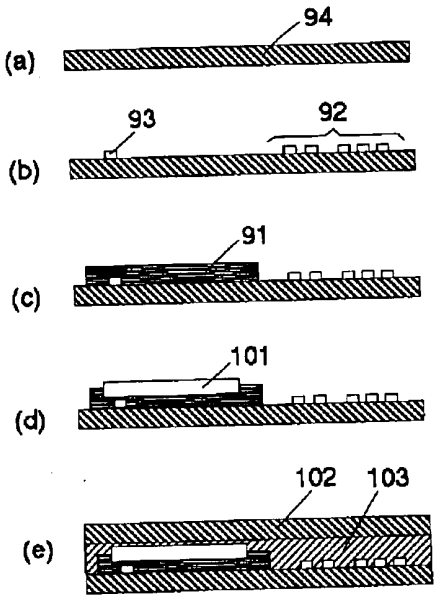
[Drawing 9]

図9



[Drawing 10]

図10



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MIYAZAKI MASARU

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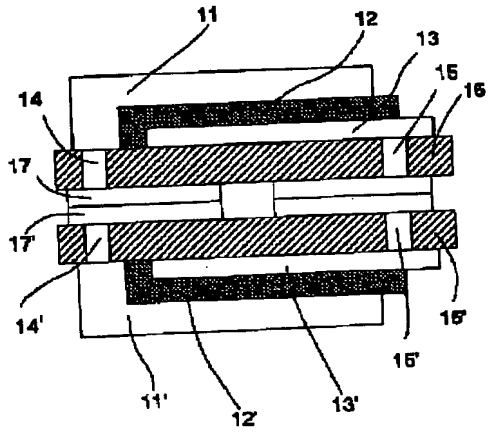
(57) Abstract:

PROBLEM TO BE SOLVED: To manufacture a laminated capacitor which is thin, high in flexual strength, and large in capacity by a method wherein a thin capacitor is composed of a first electrode layer and a second electrode layer both formed on a silicon wafer, the electrode layers are connected to junction electrodes provided in the rear of the silicon wafer through the intermediary of through-holes provided to the silicon wafer, and two of the thin capacitors are joined together by bonding the junction electrodes aligning them with each other.

SOLUTION: A thin film capacitor is composed of a first electrode layer 11 and a second electrode layer 13 both formed on the surface of a silicon wafer 16, the electrode layers 11 and 13 are connected to junction electrodes 17 provided in the rear of the wafer 16 through the intermediary of through-holes 14 and 15 provided to the wafer 16, and the two thin film capacitor of the same structure are joined together joining the junction electrodes 17 together aligning them with each other. That is, the thin capacitor is composed of the upper electrode layer 11, a dielectric layer 12, and a lower electrode layer 13, the electrode layers 11 and 13 are connected to the junction electrodes 17 provided in the rear of the silicon wafer 16 through the intermediary of the through-holes 14 and 15, and the thin capacitors of the same structure are joined together into a two-layered thin film laminated capacitor by bonding the junction electrodes 17 of them together.



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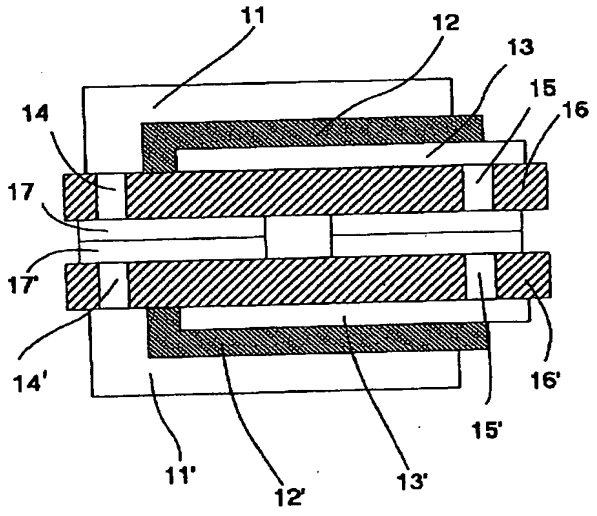
(54)【発明の名称】　薄型積層コンデンサ

(57)【要約】
【課題】　従来のセラミックコンデンサを５０ミクロン程度まで薄くすると簡単に応力で割れてしまい、薄型で大容量のコンデンサがなかった。
【解決手段】　ウエハ上にコンデンサを作製して積層する。ウエハを薄くして金属の固相拡散接合似よって接合する。上下の貫通孔はシリコンを薄くしてエッチングで開ける。
【効果】　薄型で曲げに強い大容量のコンデンサを製造することができる。

図1



【特許請求の範囲】
【請求項１】シリコンウエハ主面上に第１の電極層と第２の電極層をもっていて第１の電極層と第２の電極層の間には誘電体層があって、第１の電極層と第２の電極層はそれぞれシリコンウエハに開けられた貫通孔によってシリコン裏面に接合電極がそれぞれとられる構造の薄型コンデンサがあって他の同様の構造をもつ薄型コンデンサの接合電極とが位置合わせされて接合することを特徴とする薄型積層コンデンサ。
【請求項２】シリコンウエハ主面上に第１の電極層と第２の電極層をもっていて第１の電極層と第２の電極層の間には誘電体層があって、第１の電極層と第２の電極層はそれぞれシリコンウエハに開けられた貫通孔によってシリコン裏面に下部接合電極がそれぞれとられる構造で同様に主面の表面にも第１の電極層と第２の電極層に接続される上部接合電極をもつ構造の薄型コンデンサがあって他の同様の構造をもつ薄型コンデンサの接合電極とが位置合わせされてひとつの薄型コンデンサの下部電極と別の薄型コンデンサの上部電極が接合することを特徴とする薄型積層コンデンサ。
【請求項３】薄型コンデンサの接合電極はあらかじめアルゴンの中性原子によって表面をクリーニングしたのち接合されることを特徴とする請求項１および請求項２の薄型積層コンデンサ。
【請求項４】上記の主面側の構造はシリオコンオンインシュレータウエハを用いて形成された後、シリコンオンインシュレータの内層酸化膜層を境界にして薄くされることを特徴とする請求項１または請求項２の薄型積層コンデンサ。
【請求項５】前記の誘電体層はバリウムストロンチウム酸化チタンまたはＰＺＴによって形成されことを特徴とする請求項１または請求項２の薄型積層コンデンサ。
【請求項６】積層するコンデンサは一枚のウエハを分割して積層することを特徴とする請求項２の薄型積層コンデンサ。
【請求項７】同一の層数のコンデンサを積層して２倍の層数とする請求項２の薄型積層コンデンサ。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は薄型で曲げに強い積層コンデンサに関する発明である。
【０００２】
【従来の技術】従来技術は電子情報通信ハンドブック（オーム社発行１９９０年４月３０日第１版第２刷発行）５１６から５１７ページなどに記されている。この構造を図３に示す。この構造では酸化チタンなどを主材料とする誘電体セラミクスを焼結して図３の例では第１セラミック層３２、第２セラミック層３３、第３セラミック層３４を多層に積層した断面図のようになっている。左右には電極３１と別の電極３５が取り付けられている。
【０００３】
【発明が解決しようとする課題】この各層のセラミックの厚さは５０ミクロン程度まで薄くすることは可能であるがセラミックは粗い粒子が結合しているため極めて欠陥密度が大きくわずかな点圧などで簡単に割れてしまう。従って厚さが２００ミクロン以下を要求される薄型ＩＣカードでは曲げに耐えることができない。
【０００４】
【課題を解決するための手段】上記の課題を解決する第１の手段はシリコンウエハ主面上に第１の電極層と第２の電極層をもっていて第１の電極層と第２の電極層の間には誘電体層があって、第１の電極層と第２の電極層はそれぞれシリコンウエハに開けられた貫通孔によってシリコン裏面に接合電極がそれぞれとられる構造の薄型コンデンサがあって他の同様の構造をもつ薄型コンデンサの接合電極とが位置合わせされて接合することを特徴とする薄型積層コンデンサとすることである。
【０００５】上記の課題を解決する第２の手段はシリコンウエハ主面上に第１の電極層と第２の電極層をもっていて第１の電極層と第２の電極層の間には誘電体層があって、第１の電極層と第２の電極層はそれぞれシリコンウエハに開けられた貫通孔によってシリコン裏面に下部接合電極がそれぞれとられる構造で同様に主面の表面にも第１の電極層と第２の電極層に接続される上部接合電極をもつ構造の薄型コンデンサがあって他の同様の構造をもつ薄型コンデンサの接合電極とが位置合わせされてひとつの薄型コンデンサの下部電極と別の薄型コンデンサの上部電極が接合することを特徴とする薄型積層コンデンサとすることである。
【０００６】上記の課題を解決する第３の手段は薄型コンデンサの接合電極はあらかじめアルゴンの中性原子によって表面をクリーニングしたのち接合されることを特徴とする請求項１および請求項２の薄型積層コンデンサとすることである。
【０００７】上記の課題を解決する第４の手段は上記の主面側の構造はシリオコンオンインシュレータウエハを用いて形成された後、シリコンオンインシュレータの内層酸化膜層を境界にして薄くされることを特徴とする請求項１または請求項２の薄型積層コンデンサとすることである。
【０００８】上記の課題を解決する第５の手段は前記の誘電体層はバリウムストロンチウム酸化チタンまたはＰＺＴによって形成されことを特徴とする請求項１または請求項２の薄型積層コンデンサとすることである。
【０００９】上記の課題を解決する第６の手段は積層するコンデンサは一枚のウエハを分割して積層することを特徴とする請求項２の薄型積層コンデンサとすることである。　上記の課題を解決する第７の手段は同一の層数のコンデンサを積層して２倍の層数とする請求項２の薄

型積層コンデンサとすることである。

【００１０】

【発明の実施の形態】図１は本発明の実施例を示している。図１では二枚の薄型コンデンサを向かい合わせ接合した断面図を示している。コンデンサは上部電極層１１と誘電体層１２と下部電極層１３からなっている。上部電極層は上部電極スルーホール１４によって、また下部電極層は下部電極スルーホール１５によってシリコン１６の裏面に接合電極１７として取り出される。この接合電極同士を接続することによって２層の薄型積層コンデンサが形成される。シリコンの厚さは０．１ミクロンメートルから５０ミクロンメートル程度である。一般的にこのことを述べると、シリコンウエハ主面上に第１の電極層と第２の電極層をもっていて第１の電極層と第２の電極層の間には誘電体層があって、第１の電極層と第２の電極層はそれぞれシリコンウエハに開けられた貫通孔によってシリコン裏面に接合電極がそれぞれとられる構造の薄型コンデンサがあって他の同様の構造をもつ薄型コンデンサの接合電極とが位置合わせされて接合することを特徴とする薄型積層コンデンサとなる。基材がきわめて純度の高いシリコンを使用するので曲げに強いコンデンサが製造可能となる。

【００１１】図２は本発明の別の実施例を示している。薄型コンデンサは図１と同様に上部電極層２５と誘電体層２６と下部電極層２３からなっている。上部電極層はシリコン部スルーホール２９によって、また下部電極層はスルーホールによってシリコン２８の裏面に下部接合電極２９ａして取り出される。上部電極層２５は上部電極上部スルーホール２１によって上部接合電極２２に、下部電極層は下部電極上部スルーホール２７によって上部接合電極へ取り出される。下部接合電極２９ａは別の薄型コンデンサの別の上部接合電極に位置合わせして接合される。この接合電極同士を接続することによって２層の薄型積層コンデンサが形成される。このことを一般的に述べるとシリコンウエハ主面上に第１の電極層と第２の電極層をもっていて第１の電極層と第２の電極層の間には誘電体層があって、第１の電極層と第２の電極層はそれぞれシリコンウエハに開けられた貫通孔によってシリコン裏面に下部接合電極がそれぞれとられる構造で同様に主面の表面にも第１の電極層と第２の電極層に接続される上部接合電極をもつ構造の薄型コンデンサがあって他の同様の構造をもつ薄型コンデンサの接合電極とが位置合わせされてひとつの薄型コンデンサの下部電極と別の薄型コンデンサの上部電極が接合することを特徴とする薄型積層コンデンサとなる。

【００１２】図４は発明の実施するための工程フローを示している。図４（ａ）では酸化膜付きシリコンウエハ上に下部電極層を付けた工程直後の断面図を示す。図４（ｂ）では誘電体層を付着した工程直後の断面図を示す。この誘電体層はバリウムストロンチウム酸化チタンまたはＰＺＴによって形成されことを特徴とする。本発明のバリウムストロンチウム酸化チタン膜またはＰＺＴ膜はそれぞれ０．０１ミクロンから１０ミクロンの間であれば、通常のカードのまげ、すなわちカードの長手方向で２０センチの変位を許す曲げがあっても特性を変えることはない。図４（ｃ）では上部電極層を付着した工程直後の断面図を示す。図４（ｄ）はシリコンウエハを薄くした工程直後の断面図を示す。ウエハはシリオコンオンインシュレータウエハを用いて形成された後、シリコンオンインシュレータの内層酸化膜層を境界にして薄くすると０．１ミクロンメートルまで安定に薄くすることができる。エッチッグ液に水酸化カリウムを用いるとシリコンのみを選択的にエッチングすることができるからである。図４（ｅ）では薄くしたシリコンウエハ４５にエッチングによって下部電極スルーホール４６と下部電極スルーホール４７を開口した断面図を示している。図４（ｆ）は上部電極層接合電極４８と下部電極接合電極４９を形成した断面図を示している。

【００１３】図５は本発明の接合する工程を示している。上側の薄型コンデンサ５１と下側の薄型コンデンサ５３は中性アルゴン原子５２によって薄型コンデンサの接合電極はあらかじめアルゴンの中性原子によって表面をクリーンニングしたのち接合される。このようにすると接着層が０．１ミクロンから１ミクロンと極めて薄くできて積層コンデンサにしても厚くならない。また、室温で接着することができるので、熱膨張による収縮がなく、信頼性にすぐれた積層コンデンサを実現することができる。

【００１４】図６は本発明の実施の形態例を示している。図６（ａ）は薄型コンデンサ付きウエハ上面図６１と薄型コンデンサ付きウエハ平面図６２を示している。図６（ｂ）はウエハを２つ折して接合したコンデンサの平面図６３と断面図６４を示している。図６（ｃ）はさらに４つ折して接合したコンデンサの平面図６５と断面図６６を示している。積層するコンデンサは一枚のウエハを分割して積層することを特徴とする薄型積層コンデンサと同一の層数のコンデンサを積層して２倍の層数とする薄型積層コンデンサが可能となる。

【００１５】図７は本発明をフレキシブルなＩＣカードに搭載した実施例を示す。図７（ａ）は積層コンデンサ７１と０．１から２００μｍの薄型のコイル７４と０．１から２００μｍの薄型半導体チップ７６をカード基板７５の中立面７２に挿入して曲げた基板といっしょにこれらの積層コンデンサ７１と０．１から２００μｍの薄型のコイル７４と０．１から２００μｍ薄型半導体チップ７６が曲がるよう搭載するカードの断面図を示している。図７（ｂ）は図７（ａ）の平面図を示している。

【００１６】図８は図１の断面で示す本発明実施例の上面図を示している。

【００１７】図９は本発明の積層コンデンサをバッテリ

レスの無線カードに搭載したものを示し、図９（ａ）は平面図であり、図９（ｂ）は図９（ａ）の断面図を示す。スルーホール９６はコイルパターン９８とつなぎパターン９５をショートするための穴を示しており、コイル引出パターン９７へ電極が引き出される。このコイルパターンは銀ペーストのスクリーン印刷やエッチング技術によって形成される。

【００１８】導電性接着剤９１は積層コンデンサの上部電極１１とコイル接続端子９３を接続するものである。導電性接着剤は絶縁材料に導電性微粒子を分散した異方性導電接着剤であってもよい。カード基板９４の上には、印刷的手法により形成されたコイル部分９２が存在する。

【００１９】図１０はコイルやコンデンサをカードに組み込む工程の断面を示したものである。図１０（ａ）はカード基板の断面を示している。図１０（ｂ）は銀ペーストなどの導電材料をスクリーン印刷などによってコイルパターンを印刷した断面を示している。図１０（ｃ）は導電性接着材を印刷した直後の工程の断面を示している。図１０（ｄ）は積層コンデンサ１０１を接着した工程直後の断面をしめしている。この積層コンデンサ１０１の構造はたとえば図１に示す積層コンデンサと同じような構造を持つものである。図１０（ｅ）は接着剤１０３によりカードカバーシート１０２を接着して完成したカードの工程直後の断面を示す。

【００２０】

【発明の効果】本発明は請求項１の通りシリコンウエハ主面上に第１の電極層と第２の電極層をもっていて第１の電極層と第２の電極層の間には誘電体層があって、第１の電極層と第２の電極層はそれぞれシリコンウエハに開けられた貫通孔によってシリコン裏面に接合電極がそれぞれとられる構造の薄型コンデンサがあって他の同様の構造をもつ薄型コンデンサの接合電極とが位置合わせされて接合することを特徴とする薄型積層コンデンサを提案している。このような構成のコンデンサによれば、厚さ１から５０ミクロン程度でも１０から１００マイクロファラッドのような大容量で薄型でかつ曲げることができるコンデンサを得ることが可能となる。これはシリコンに形成されたコンデンサを積層とする構造のために薄型で大容量が可能となり、フレキシブルＩＣカードなどの薄型カードの実現をもたらす効果がえられる。具体的に図７にフレキシブルＩＣカードの構成を示し、図９に本発明の積層コンデンサを搭載した構成を示す。このような図９の構成のカードではコイルとコンデンサによってエネルギをタンクに蓄える電気的な構成の一部をなす。このとき、コイルは印刷状に構成されるので、巻数が限定されて、大インダクタンスが実現することが困難であり、大容量で薄型のコンデンサを必要とする。このような薄型で大容量のコンデンサ付カードが実現できると、従来に比べて電磁波によるエネルギを貯めやすくなるので、従来が５から１０センチの距離のものが、バッテリレスで１５から５００センチの距離でもカードが動作できるエネルギを蓄えることが可能となり応用範囲をひろくすることができる。

【００２１】従来のセラミックコンデンサを５０ミクロン程度まで薄くすると簡単に応力で割れてしまい、薄型で大容量のコンデンサがなかった。従来のセラミックコンデンサでは曲率半径１００ミリメートルで簡単にわれてしまうが本発明の積層コンデンサでは１０ミリメートル以下になるまで割れることはなく、極めて顕著な発明効果をもたらす。本発明ではウエハ上にコンデンサを作製して積層する。ウエハを薄くして金属の固相拡散接合によって接合する。上下の貫通孔はシリコンを薄くしてエッチングで開けることにより薄型で曲げに強い大容量のコンデンサを製造することができる効果を出すことができた。

【００２２】本発明の積層コンデンサは小さい面積で薄型により大容量のコンデンサを実現できるので、小さい面積であるため歩留まりよく経済的に、また薄型であるので曲げにつよく薄いフレキシブルＩＣカードに向いたコンデンサ部品を提供することができる。

【図面の簡単な説明】

【図１】本発明の実施例を示す。

【図２】本発明の別の実施例を示す。

【図３】従来のコンデンサの構造を示す。

【図４】本発明の実施フローを示す。

【図５】本発明の実施フローを示す。

【図６】ウエハから積層コンデンサを作製する方法を示す。

【図７】本発明の別の実施例を示す。

【図８】本発明の別の実施例を示す。

【図９】本発明の別の実施例を示す。

【図１０】本発明の別の実施例を示す。

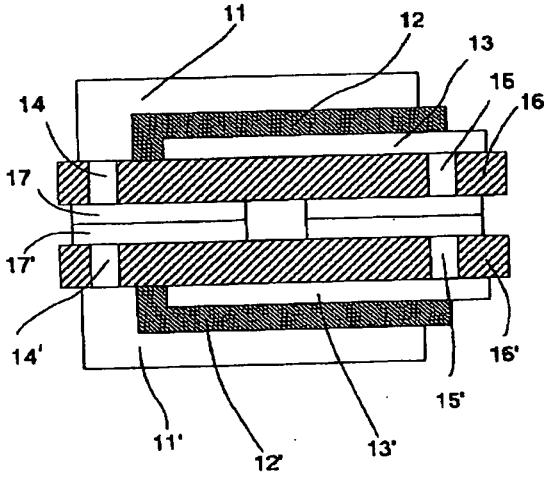
【符号の説明】

１１…上部電極層
１２…誘電膜層
１３…下部電極層
１４…上部電極スルーホール
１５…下部電極スルーホール
１６…シリコン
１７…接合電極
２１…上部電極上部スルーホール
２２…上部接合電極
２３…下部電極層
２４…絶縁膜層
２５…上部電極層
２６…誘電膜層
２７…下部電極上部スルーホール
２８…シリコン
２９…シリコン部スルーホール

２９ａ…下部接合電極
２９ｂ…別の上部接合電極
３１…電極
３２…第１セラミック層
３３…第２セラミック層
３４…第３セラミック層
３５…別の電極
４１…酸化膜付きシリコンウエハ
４２…下部電極層
４３…誘電体層
４４…上部電極層
４５…薄くしたシリコンウエハ
４６…上部電極スルーホール
４７…下部電極スルーホール
４８…上部電極層接合電極
４９…下部電極層接合電極
５１…上側の薄型コンデンサ
５２…中性アルゴン原子
５３…下側の薄型コンデンサ
６１…薄型コンデンサ付きウエハ上面図
６２…薄型コンデンサ付きウエハ断面図
６３…二つ折したコンデンサ上面図
６４…二つ折したコンデンサ断面図
６５…四つ折したコンデンサ上面図
６６…四つ折したコンデンサ断面図
７１…積層ンデンサ
７２…中立面
７４…コイル
７５…カード基板
７６…薄型半導体チップ
９１…導電性接着剤
９２…コイル部分
９３…コイル接続端子
９４…カード基板
９５…つなぎパターン
９６…スルーホール
９７…コイル引出パターン
９８…コイルパターン
１０１…積層コンデンサ
１０２…カードカバーシート
１０３…接着剤。

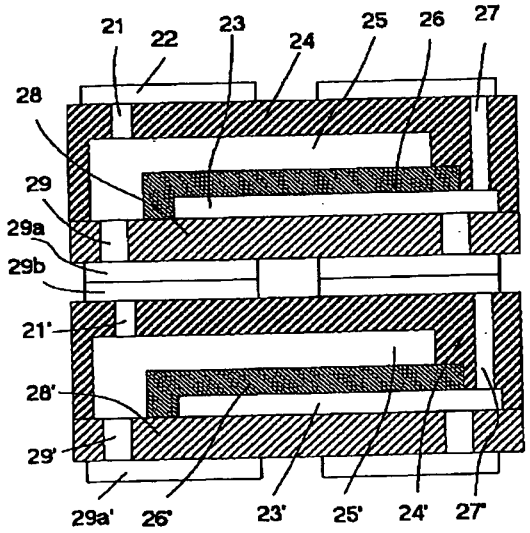
【図１】

図1



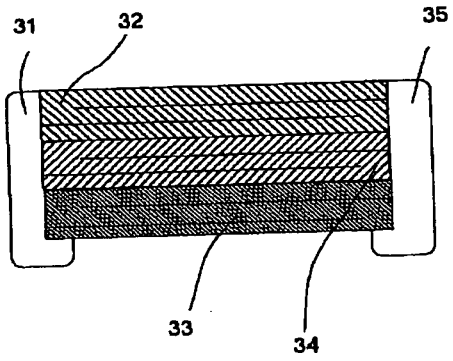
【図２】

図2



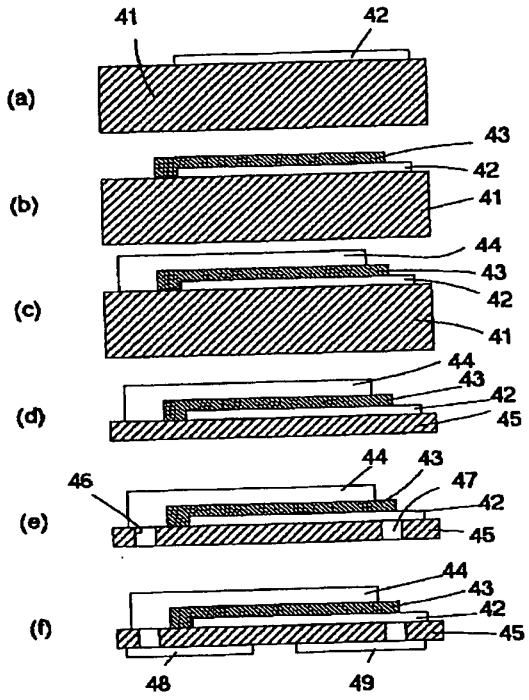
【図３】

図3



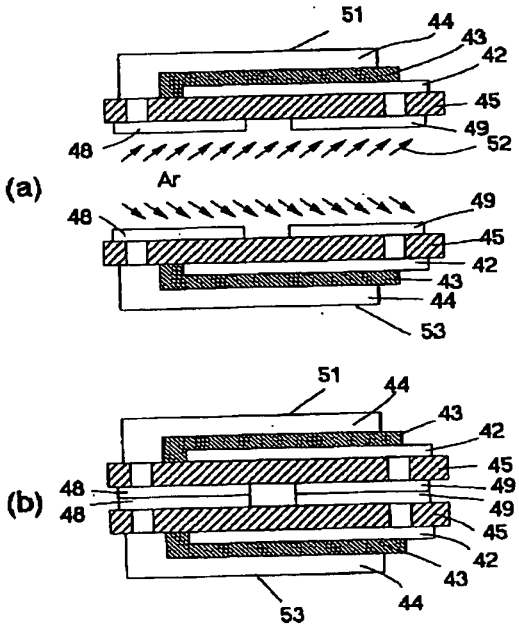
【図４】

図4



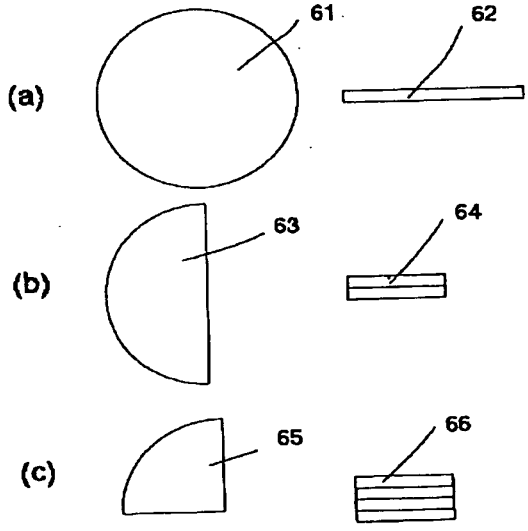
【図５】

図5



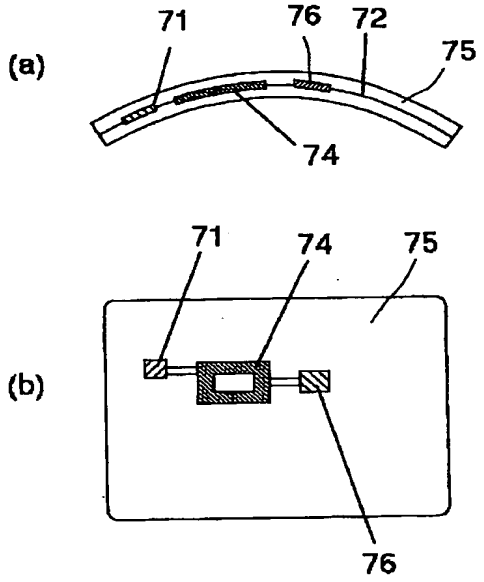
【図６】

図6



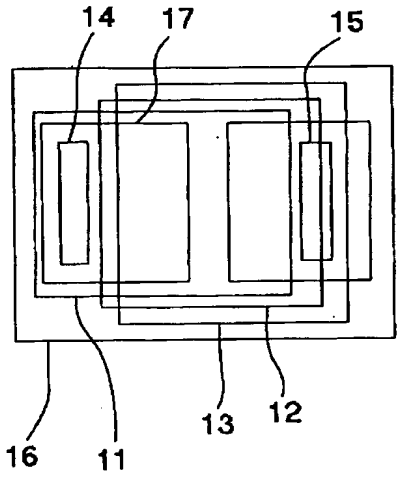
【図７】

図7



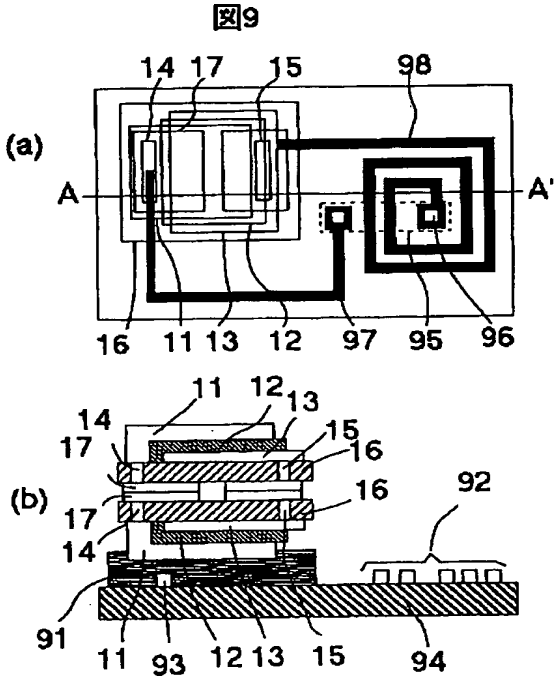
【図８】

図8



【図９】

図9



【図１０】

図10